ELECTRICAL & ELECTRONICS ENGINEERING WORKSHOP
(Common to All branches of Engineering)

PART-B

ELECTRONICS ENGINEERING LAB

(LABORATORY MANUAL)

LAB CODE: R23ES05 **SCHEME: R23**

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

BEHARA COLLEGE OF ENGINEERING & TECHNIOLOGY

Approved by AICTE. New Delhi, Affiliated to JNT University, Gurajada Vizianagaram

88th ward , Narava(V), Visakhapatnam, 530027

VISION

The Department of Electronics and Communication Engineering endeavours to develop excellence in Technical Education and Research by producing high quality, technically competent and socially responsible engineers.

MISSION

- **To foster and achieve unmatched excellence in Electronics and Communication Engineering Domain.**
- **To pursue continuous improvement in infrastructure and state-of-the art laboratories.**
- **To establish and set best teaching and learning standards among top grade Engineering Departments across the nation.**
- **To encourage learning, research, creativity, innovation and professional activity by offering ambience and support.**
- **To prepare the students to meet the global needs of Industry and Society by inculcating professional ethics.**

By the completion of Electronics & Communication engineering program, the students will be to:

PROGRAM EDUCATIONAL OBJECTIVES (PEOS):

PEO1:

Learn Core Skills, skill to understand, analyse, design, create novel products and implementation of complex systems by applying basic concepts in Electronics & Communication Engineering to Electronics, Communications, Signal processing, VLSI, Embedded Systems. (Core Skills).

PEO2:

Problem solving using hardware and software tools & Lifelong learning, Capability to pursue career in industry or higher studies with continuous learning. (Problem-Solving Skills).

PEO3:

Entrepreneurship Skills, Leadership qualities, team spirit, multi-disciplinary approach, character moulding, effective communication skills, lifelong learning and sense of responsibility towards society for a successful professional career. (Professional Career).

PROGRAM SPECIFIC OUTCOMES (PEOS):

PSO-1:

Design and implementation of complex systems by applying basic concepts in Electronics & Communication Engineering to Electronics, Communications, Signal processing, VLSI, Embedded Systems (Core Skills).

PSO-2: Solve complex Electronics and Communication Engineering problems, using hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions relevant to the society (Problem-Solving Skills).

PSO-3:

Quality in technical subjects for successful higher studies and employment (Professional Career).

PROGRAM OUTCOMES (POs)

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and nee d for sustainable development.
8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

SYLLABUS

PART B: ELECTRONICS ENGINEERING LAB

Course Objectives:

- To impart knowledge on the principles of digital electronics and fundamentals of electron devices & its applications.

Course Outcomes: At the end of the course, the student will be able to
CO1: Identify & testing of various electronic components.
CO2: Understand the usage of electronic measuring instruments.
CO3: Plot and discuss the characteristics of various electron devices.
CO4: Explain the operation of a digital circuit.

List of Experiments:

1. Plot V-I characteristics of PN Junction diode A) Forward bias B) Reverse bias.
2. Plot V – I characteristics of Zener Diode and its application as voltage Regulator.
3. Implementation of half wave and full wave rectifiers
4. Plot Input & Output characteristics of BJT in CE and CB configurations
5. Frequency response of CE amplifier.
6. Simulation of RC coupled amplifier with the design supplied
7. Verification of Truth Table of AND, OR, NOT, NAND, NOR, Ex-OR, Ex-NOR gates using ICs.
8. Verification of Truth Tables of S-R, J-K& D flip flops using respective ICs.

Tools / Equipment Required: DC Power supplies, Multi meters, DC Ammeters, DC Voltmeters,AC Voltmeters, CROs, all the required active devices.

References:

1. R. L. Boylestad & Louis Nashlesky, Electronic Devices & Circuit Theory, Pearson Education, 2021.
2. R. P. Jain, Modern Digital Electronics, 4th Edition, Tata Mc Graw Hill, 2009
3. R. T. Paynter, IntroductoryElectronic Devices & Circuits – Conventional Flow Version,Pearson Education,2009.

Note: Minimum Six Experiments to be performed. All the experiments shall be implemented using both Hardware and Software

During the lab class

Do's

1. Be punctual and regular to the laboratory.

2. Maintain Discipline all the time and obey the instructions.

3. Check the connections properly before turning ON the circuit.

4. Turn OFF the circuit immediately if you see any component heating.

5. Dismount all the components and wires before returning the kit.

6. Any failure / break-down of equipment must be reported to the faculty

Don'ts

1. Don't touch live electric wires.

2. Don't turn ON the circuit unless it is completed.

3. Avoid making loose connections.

4. Don't leave the lab without permission.

5. Do not handle any equipment without reading the instructions/Instruction

Manuals

ABOUT THE LAB

In this lab students will be able to study and analyses the basic electronic devices like diodes, BJTs, JFETs, Half-wave & full-wave rectifiers. Rectifiers are introduced and their performances with different types of filters are observed and basic amplifiers. With this knowledge students will be able to do mini-projects with the help of diodes and transistors.

SIGNIFICANCE OF THE LAB

Electronics laboratory is used for examining operating principles of the electronic devices and obtaining the characteristics of electronic circuit components. Design and practical applications of power supplies, amplifiers, oscillators and various digital electronic circuits in various Industries and Production Houses.

The Basic Electronics Lab is designed to teach students about the different types of analog and digital electronics circuitry under courses like Basic Electronics Laboratory, Analog Circuit Laboratory as well as Analog Integrated Circuit Laboratory.

Course Designed by	Department of Electronics and Communication Engineering
Category	• Discrete based Experiments (DBE)
	• Simulation based Experiments (SBE)
Broad Area of Syllabus	ELECTRONICS DEVICES LABORATORY

EXP No:-1

V-I CHARACTERISTICS OF PN JUNCTION DIODE

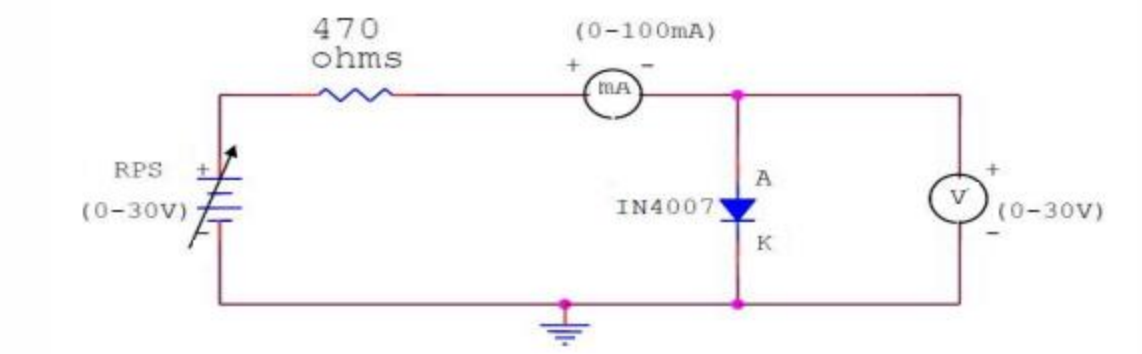
AIM: To plot the V-I characteristics of PN junction diode in forward and reverse bias and also to calculate Static and Dynamic Resistance.

APPARATUS:

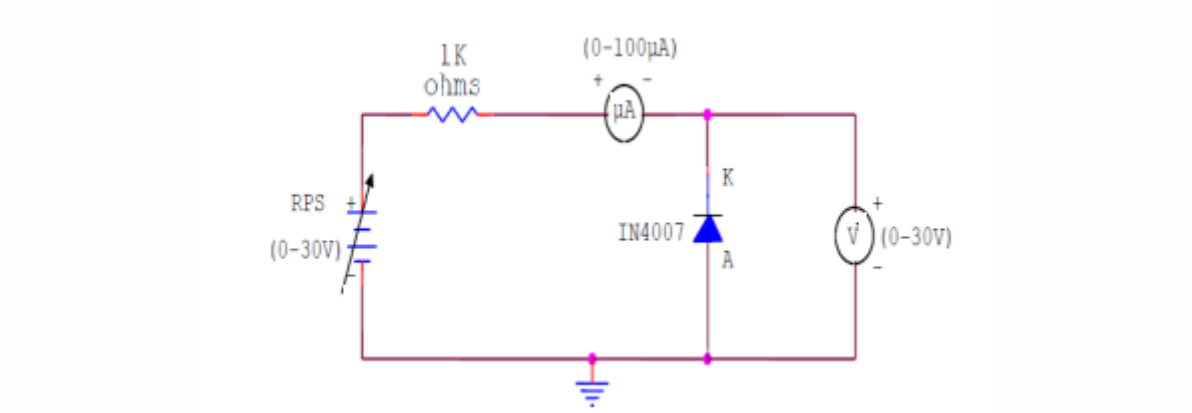
1. 1N4007Diode.
2. Resistor 470Ω,1KΩ.
3. Ammeter(0-100mA), (0-100µA).
4. Voltmeter (0- 30V).
5. RPS (0-30V)
6. BreadBoard with connecting wires.

CIRCUIT DIAGRAM:

Forward Bias :



Reverse Bias:



TABULARFORMS:

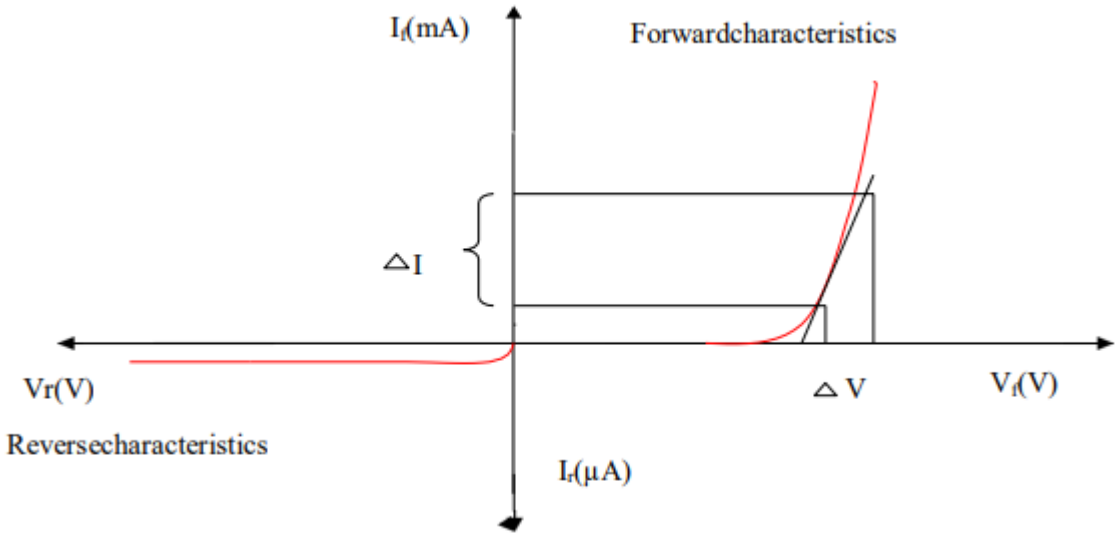
Forward Bias:

S NO	V_S (Volts)	V_f (Volts)	I_f (mA)

Reverse Bias:

S NO	V_S (Volts)	V_r (Volts)	I_r (µA)

Model Graph:



THEORY: - A p-n junction diode conducts only in one direction. The V-I characteristics of the diode are curve between voltage across the diode and current through the diode. When external voltage is zero, circuit is open and the potential barrier does not allow the current to flow. Therefore, the circuit current is zero.

When P-type (Anode is connected to +ve terminal and n- type (cathode) is connected to –ve terminal of the supply voltage, is known as forward bias. The potential barrier is reduced when diode is in the forward biased condition. At some forward voltage, the potential barrier altogether eliminated and current starts flowing through the diode and also in the circuit. The diode is said to be in ON state. The current increases with increasing forward voltage.

When N-type (cathode) is connected to +ve terminal and P-type (Anode) is connected to –ve terminal of the supply voltage is known as reverse bias and the potential barrier across the junction increases. Therefore, the junction resistance becomes very high and a very small current (reverse saturation current) flows in the circuit. The diode is said to be in OFF state. The reverse bias current due to minority charge carriers

PROCEDURE:

(i) FORWARD BIAS (For 'Ge' and 'Si' Diode):

1. Connections are made as per the circuit diagram.
2. For forward bias, the RPS +ve is connected to the anode of the diode and RPS –ve is connected to the cathode of the diode,
3. Switch ON the power supply and increases the input voltage (supply voltage) in Steps.
4. Note down the corresponding current flowing through the diode and voltage across the diode for each and every step of the input voltage.
5. The readings of voltage and current are tabulated.
6. Graph is plotted between voltage on x-axis and current on y-axis

(ii) REVERSE BIAS :

1. Connections are made as per the circuit diagram.
2. For reverse bias, the RPS +ve is connected to the cathode of the diode and RPS –ve is connected to the anode of the diode.
3. Switch ON the power supply and increase the input voltage (supply voltage) in Steps.
4. Note down the corresponding current flowing through the diode and voltage across the diode for each and every step of the input voltage.
5. The readings of voltage and current are tabulated.
6. The Graph is plotted between voltage on x-axis and current on y-axis.

CALCULATIONS:

i. Static resistance = V / I

ii. Dynamic resistance=ΔV/Δ

iii. Cut in voltage=

PRECAUTIONS:

1. While doing the experiment do not exceed the ratings of the diode. This may lead to damage the diode.
2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Connections must be made carefully to avoid short circuit.
5. Readings must be taken without parallel ox error

RESULT: The V-I Characteristics of a PN-diode are observed and the graphs are plotted. And the values obtained from the graph are

1. Static resistance =
2. Dynamic resistance=
3. Cut-in Voltage =

EXP No:-2

V-I CHARACTERISTICS OF ZENER DIODE AND ZENER DIODE REGULATOR

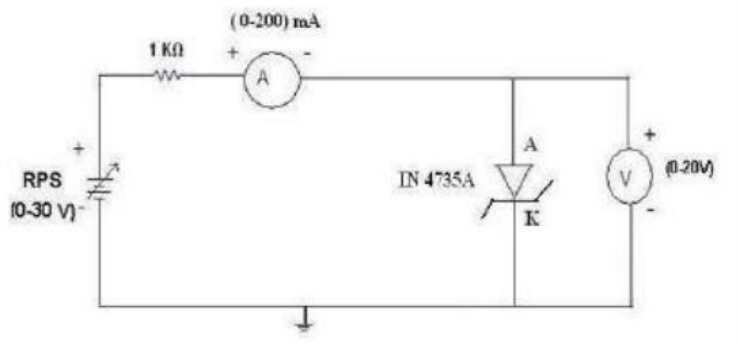
AIM: To plot the V-I characteristics of Zener Diode in reverse bias and to verify that Zener Diode acts as a Voltage Regulator.

APPARATUS:

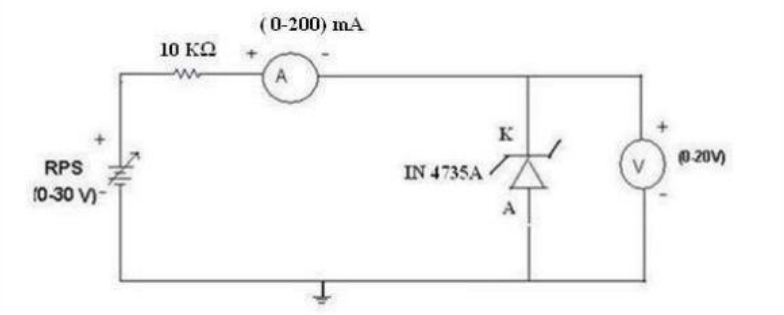
1) Zener diode IN4148 / IN4735A.
2) 470Ω,1K Ω,10K Ω resistors.
3) Ammeter (0-50mA).
4) Voltmeter(0-10V).
5) RPS(0-30V).
6) Bread Board.
7) Decade Resistance Box (DRB).
8) Connecting Wires.

CIRCUIT DIAGRAM:

Forward Bias :



Reverse Bias:



TABULARFORMS:

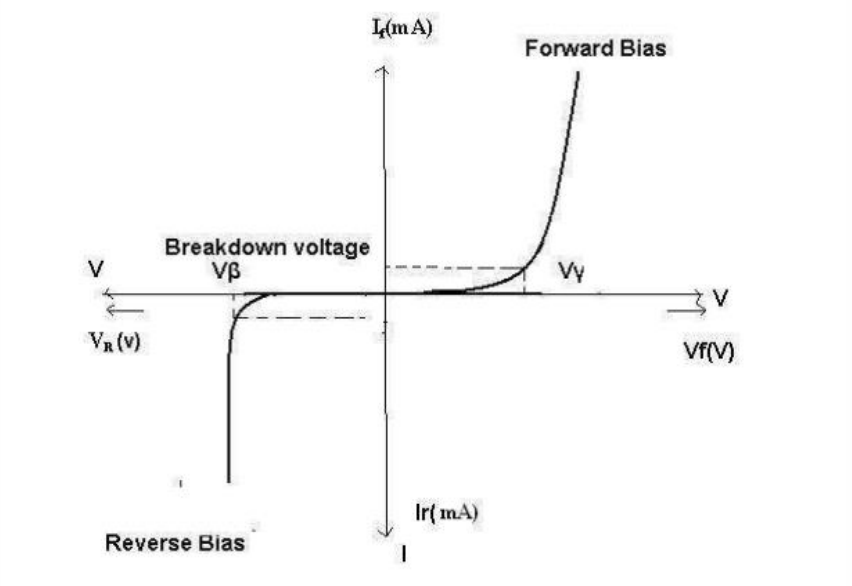
Forward Bias:

S NO	V_S (Volts)	V_f (Volts)	I_f (mA)

Reverse Bias:

S NO	V_S (Volts)	V_r (Volts)	I_r (µA)

Model Graph:



THEORY: A Zener diode is heavily doped p-n junction diode, specially made to operate in the break down region. A p-n junction diode normally does not conduct when reverse biased. But if the reverse bias is increased, at a particular voltage it starts conducting heavily. This voltage is called Break down Voltage. High current through the diode can permanently damage the device.

To avoid high current, we connect a resistor in series with Zener diode. Once the diode starts conducting it maintains almost constant voltage across the terminals whatever may be the current through it, i.e., it has very low dynamic resistance. It is used in voltage regulators.

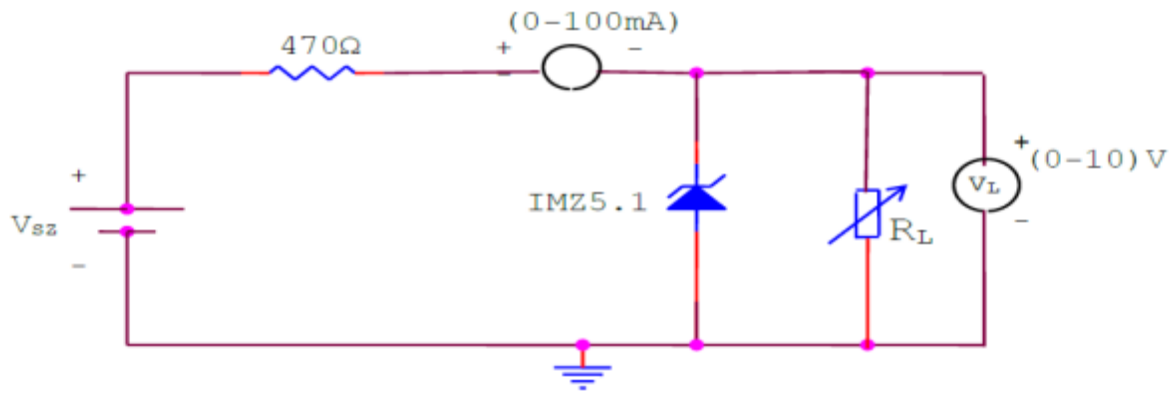
PROCEDURE:

V-I CHARACTERISTICS:

1. Connections are made as per the circuit diagram.
2. The Regulated power supply voltage is increased in steps.
3. The Zener current (lz), and the Zener voltage (Vz.) are observed and then noted in the tabular form.
4. A graph is plotted between Zener current (Iz) on y-axis and Zener voltage (Vz) on x-axis.

Zener diode as Voltage Regulator:

CIRCUIT DIAGRAM:



TABULAR FORM:(Regulation Characteristics) V_{NL}=……

S.No.	R_L(ohms)	V_L (Volts)	$I_S=(I_Z+I_L)$ (mA)	%Regulation

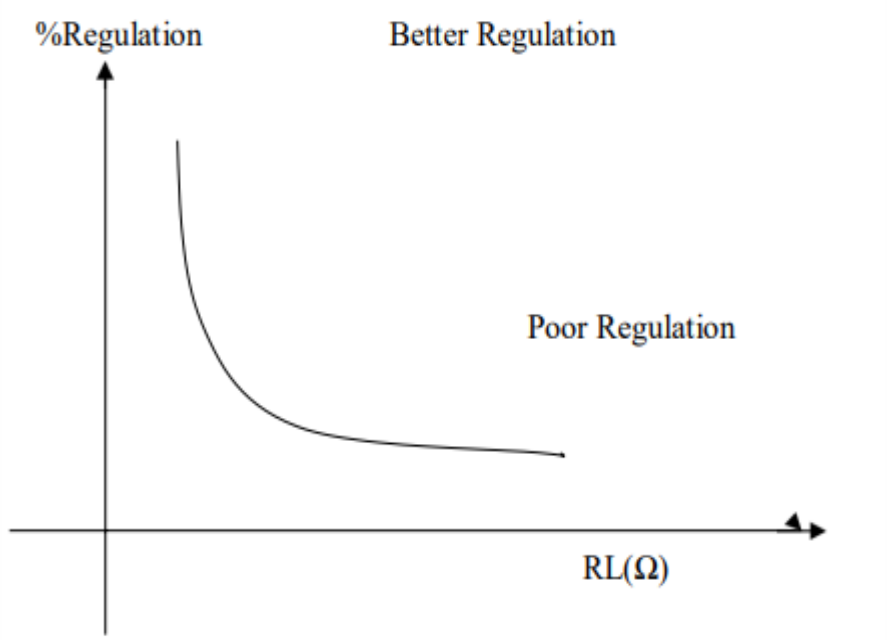
PROCEDURE:

As Voltage Regulator:

1. Make the connections as shown in figure.
2. Measure VNL (No load voltage) by opening the load resistance.
3. Connect the load resistance, and vary the load resistance from 1100Ω to 100Ω in steps of 100Ω and note down the readings of Voltmeter (V_Z)and Ammeter (I_S).
4. Calculate %Regulation by using the formula given below

$$\%\text{Regulation}=\frac{VNL-VFL}{VFL} \times 100$$

MODEL GRAPH:



PRECAUTIONS:

1. While doing the experiment do not exceed the ratings of the Zener diode. This may lead to damage the diode.
2. Connect voltmeter and Ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

RESULT:

1. The reverse bias characteristics of Zener diode are observed and the graph was plotted. And the breakdown voltage was obtained from the graph.
2. The Regulation characteristics of a Zener Diode are observed and the graph was plotted.

EXP No-3

FULL WAVE RECTIFIER WITH AND WITHOUT FILTERS

AIM: 1. To obtain the load regulation and ripple factor of a full-wave rectifier by using (a). without Filter (b). with Filter

2. To observe the input and output waveforms of a full-wave rectifier.

APPARATUS:

1 Diodes IN 4007 (Si)	2
2 Decade Resistance Box (1KΩ-10 KΩ)	1
3 Transformer 230 V AC	1
4 Capacitor 100μF	1
5 Bread Board	1
6 Digital Voltmeter (0-20) V (AC & DC)	2
7 Connecting Wires	as Require

THEORY:

A device is capable of converting a sinusoidal input waveform into a unidirectional waveform with non-zero average component is called a rectifier. A practical half wave rectifier with a resistive load is shown in the circuit diagram. During the positive half cycle of the input the diode conducts and all the input voltage is dropped across RL. During the negative half cycle the diode is reverse biased and it acts as almost open circuit so the output voltage is zero.

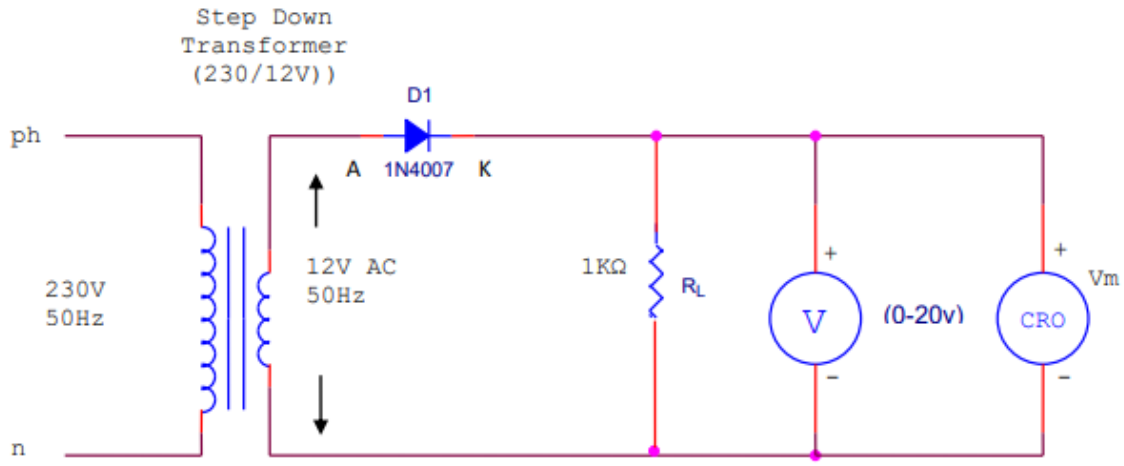
The filter is simply a capacitor connected from the rectifier output to ground. The capacitor quickly charges at the beginning of a cycle and slowly discharges through RL after the positive peak of the input voltage. The variation in the capacitor voltage due to charging and discharging is called ripple voltage. Generally, ripple is undesirable, thus the smaller the ripple, the better the filtering action.

Full wave rectifier: The full wave rectifier consists of two half wave rectifiers connected to a common load. One rectifies during positive half cycle of the input and the other rectifying the negative half cycle. The transformer supplies the two diodes (D1 and D2) with sinusoidal input voltages that are equal in magnitude but opposite in phase. During input positive half cycle, diode D1 is ON and diode D2 is OFF. During negative half cycle D1 is OFF and diode

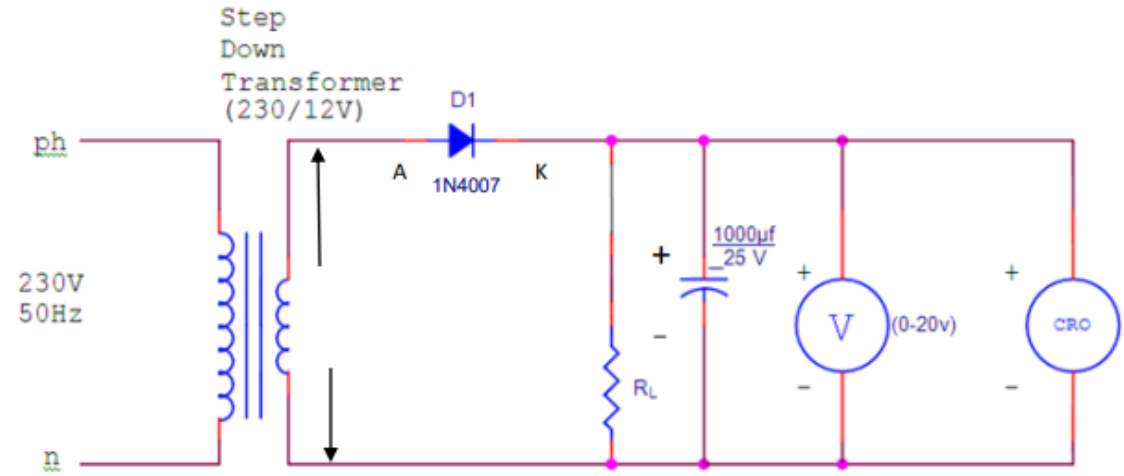
D2 is ON. Generally, ripple is undesirable, thus the smaller the ripple, the better the filtering action.

CIRCUIT DIAGRAM:

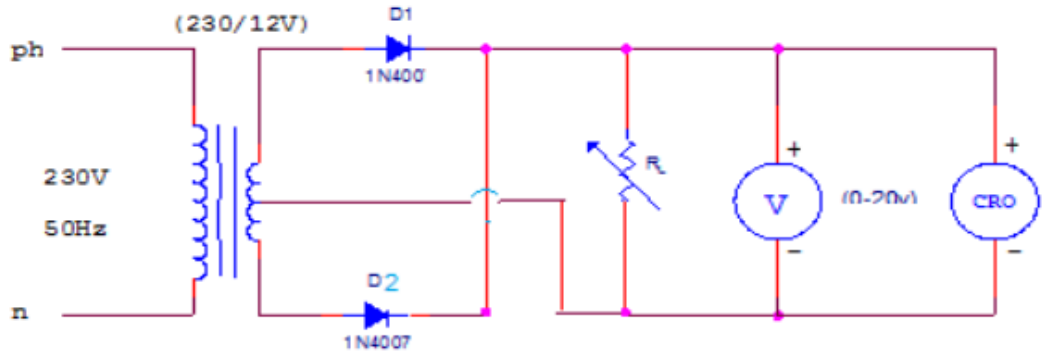
Halfwave Rectifier without filter



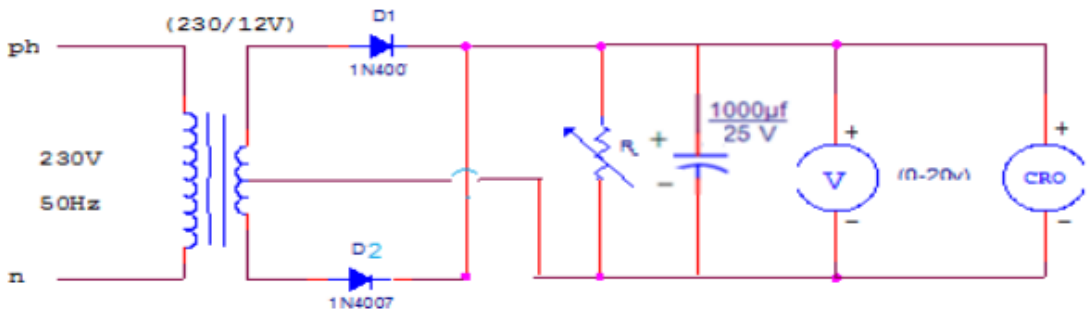
Half wave Rectifier with Capacitor Filter



Full wave Rectifier without Filter



Full wave Rectifier with capacitor Filter



CALCULATIONS:

Theoretical calculations for Ripple factor of Halfwave Rectifier: - Without Filter: -

Vdc=

Vrms=

Ripple factor=

Theoretical calculations for Ripple factor of Halfwave Rectifier: - With Filter: -

Vdc=

Vrms=

Ripple factor=

Theoretical calculations for Ripple factor of fullwave Rectifier: - Without Filter: -

Vdc=

Vrms=

Ripple factor=

Theoretical calculations for Ripple factor of fullwave Rectifier: - With Filter: -

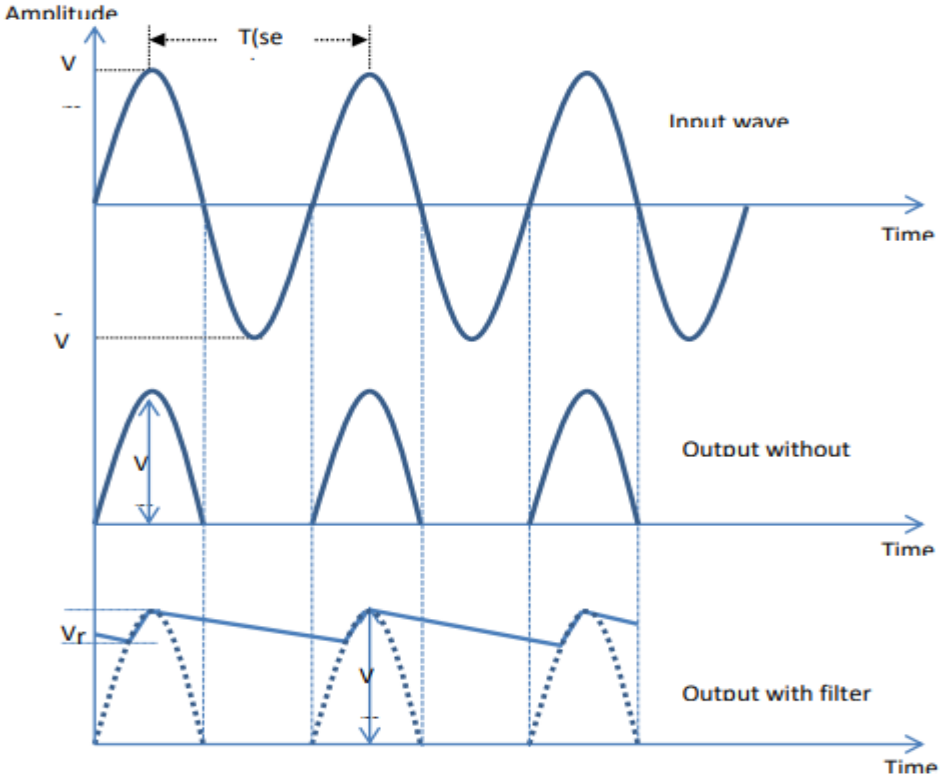
Vdc=

Vrms=

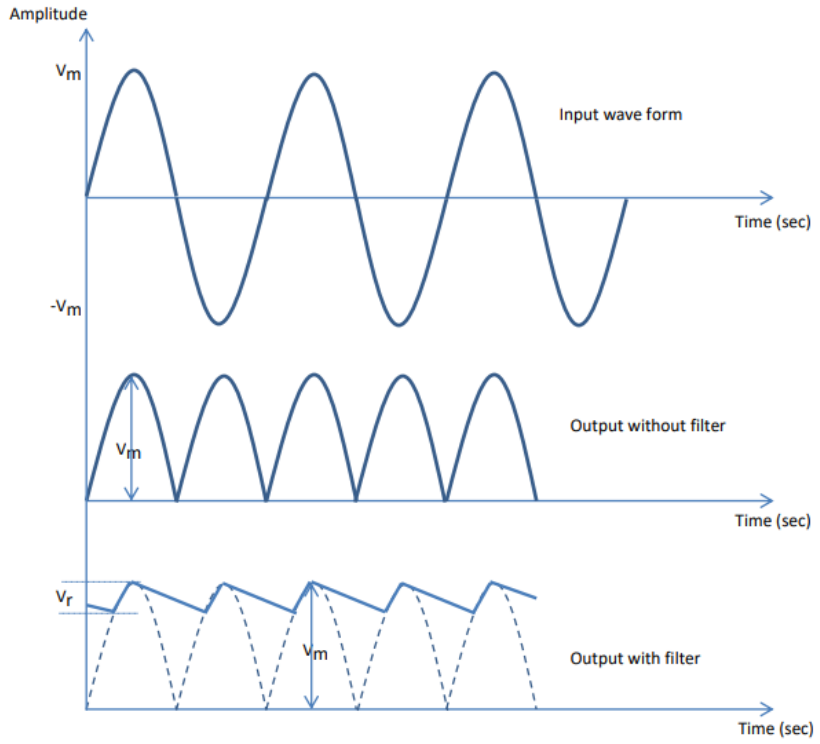
Ripple factor=

Model Graphs:

Half Wave Rectifier:



Fullwave Rectifier:



Procedure :

HWR Without Filter:

1. Connections are made as per the circuit diagram of the rectifier without filter.
2. Connect the primary side of the transformer to ac mains and the secondary side to the rectifier input.
3. Note down the no load voltage before applying the load to the Circuit and by using the Multimeter, measure the ac input voltage of the rectifier and its frequency.
4. Now Vary the RL in steps of 100Ω by varying the DRB from 1100Ω to 100Ω and note down the load voltage (VL) using the multimeter for each value of RL and calculate the percentage regulation.
5. Measure the AC and DC voltage at the output of the rectifier for each value of RL using Multimeter.
6. Now Observe the output waveform on CRO across RL and find out value of Vm.
7. Now calculate Vdc, Vrms, Ripple Factor and other parameters of half wave rectifier according to the given formulae.
8. Measure the amplitude and time period of the transformer secondary (input waveform) by connecting CRO.
9. Feed the rectified output voltage to the CRO and measure the time period and amplitude of the waveform.

HWR With Capacitor Filter:

1. Connections are made as per the circuit diagram of the rectifier with filter.
2. Connect the primary side of the transformer to ac mains and the secondary side to the rectifier input.
3. By the multimeter, measure the ac input voltage of the rectifier and, ac and dc voltage at the output of the rectifier.
4. Measure the amplitude and time period of the transformer secondary (input waveform) by connecting CRO.
5. Feed the rectified output voltage to the CRO and measure the time period and amplitude of the waveform.

FWR Without Capacitor Filter:

1. Connections are made as per the circuit diagram of the rectifier without filter.
2. Connect the primary side of the transformer to ac mains and the secondary side to the rectifier input.
3. By the multimeter, measure the ac input voltage of the rectifier and, ac and dc voltage at the output of the rectifier.

4. Measure the amplitude and time period of the transformer secondary (input waveform) by connecting CRO.
5. Feed the rectified output voltage to the CRO and measure the time period and amplitude of the Waveform.

FWR With Capacitor Filter:

1. Connections are made as per the circuit diagram of the rectifier with filter.
2. Connect the primary side of the transformer to ac mains and the secondary side to the rectifier input.
3. By the multimeter, measure the ac input voltage of the rectifier and, ac and dc voltage at the output of the rectifier.
4. Measure the amplitude and time period of the transformer secondary (input waveform) by connecting CRO.
5. Feed the rectified output voltage to the CRO and measure the time period and amplitude of the waveform.

PRECAUTIONS :

1. The primary and secondary sides of the transformer should be carefully identified.
2. 2. The polarities of the diode should be carefully identified.

RESULT: The input and output waveforms of half wave rectifier and full wave rectifier are is plotted .

Ripple factor of HWR without Filter =

Ripple factor of HWR with Capacitor Filter =

The input and output waveforms of full wave rectifier are is plotted .

Ripple factor of FWR without Filter =

Ripple factor of FWR with Capacitor Filter =

EXP NO:04

INPUT & OUTPUT CHARACTERISTICS OF BJT IN CE AND CB CONFIGURATIONS

CB CHARACTERSTICS OF A TRANSISTOR

AIM: To obtain the input and output characteristics of a transistor connected in common base configuration

APPARATUS:

1.NPN-Transistor	- BC107
2.Regulated Power supply	-(0-15V)
3.Resistor	-1KΩ
4.Ammeter	-(0-200mA)
5.Voltmeter	-(0-20V)
6.Breadboard	
7.Connecting wires	

THEORY: A transistor is a three terminal active device. The terminals are emitter, base, collector. In CB configuration, the base is common to both input (emitter) and output (collector). For normal operation, the E-B junction is forward biased and C-B junction is reverse biased.

In CB configuration, I_E is +ve, IC is –ve and I_B is –ve. So,

$$\mathbf{V_{EB} = f1\ (V_{CB}, I_E)\ and}$$

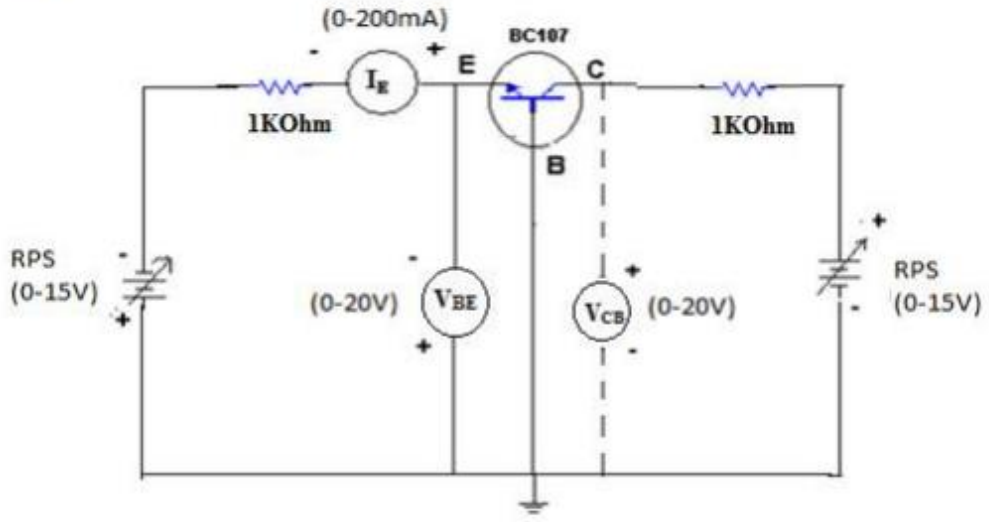
$$\mathbf{I_C = f2\ (V_{CB}, I_E)}$$

With an increasing the reverse collector voltage, the space-charge width at the output junction increases and the effective base width (W) decreases. This phenomenon is known as “Early effect”. Then, there will be less chance for recombination within the base region. With increase of charge gradient with in the base region, the current of minority carriers injected across the emitter junction increases. The current amplification factor of CB configuration is given by,

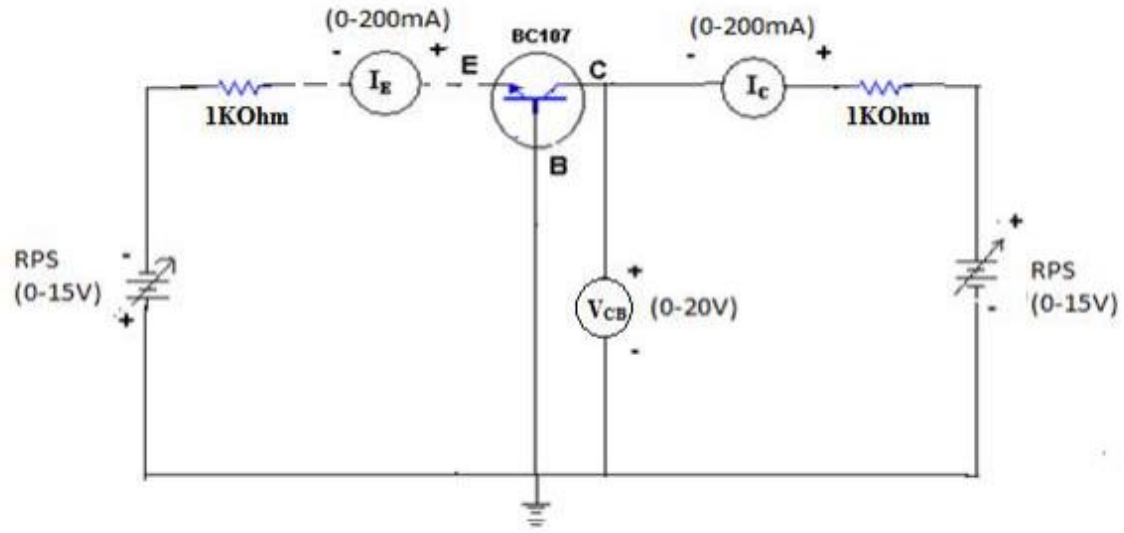
$$\alpha = \Delta I_C / \Delta I_E$$

CIRCUIT DIAGRAM:

INPUT CHARACTERSTICS:



OUTPUT CHARACTERSTICS:



PROCEDURE:

INPUT CHARACTERISTICS:

1. Connections are made as per the circuit diagram.

2. For plotting the input characteristics, the output voltage VCB is kept constant at 0V and for different values of VBE note down the values of IE.

3. Repeat the above step keeping VCB at 5V, 10V. All the readings are tabulated.

4. A graph is drawn between VBE and IE for constant VCB.

OUTPUT CHARACTERISTICS:

1. Connections are made as per the circuit diagram.

2.For plotting the output characteristics, the input IE is kept constant at 1mA and for different values of VCB, note down the values of IC.

3. Repeat the above step for the values of IE at 2 mA, and 3 mA, all the readings are tabulated.

4. A graph is drawn between VCB and IC for constant IE

OBSERVATIONS:

INPUT CHARACTERISTICS:

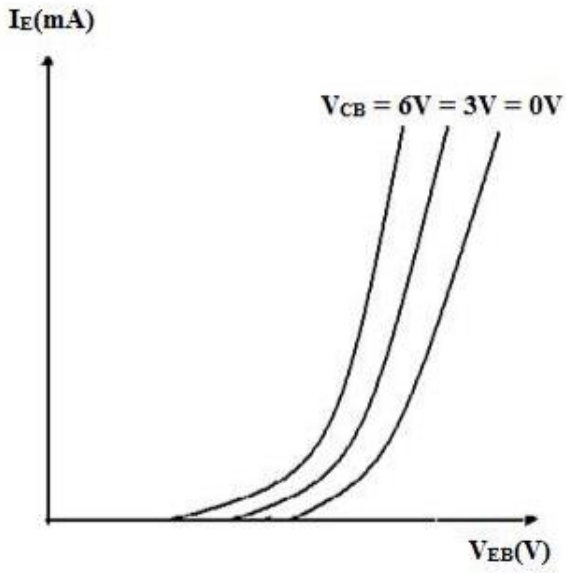
S.No	$V_{CB}=0V$		$V_{CB}=3V$		$V_{CB}=6V$	
	$V_{EB}(V)$	$I_E(mA)$	$V_{EB}(V)$	$I_E(mA)$	$V_{EB}(V)$	$I_E(mA)$

OUTPUT CHARACTERISTICS:

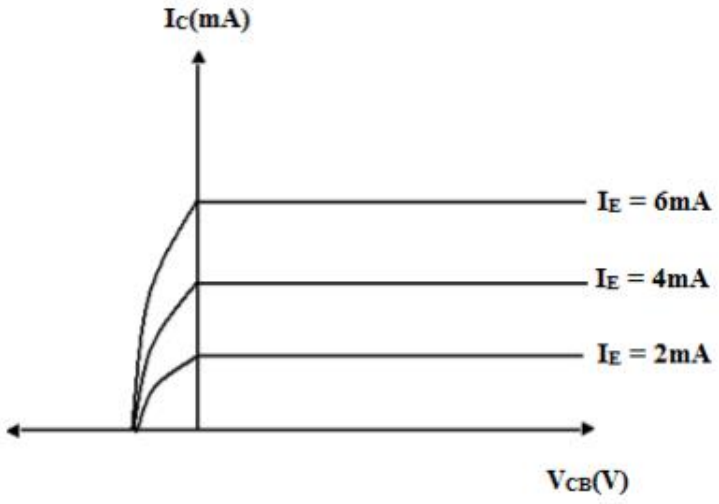
S.No	$I_E=2mA$		$I_E=4mA$		$I_E=6mA$	
	$V_{CB}(V)$	$I_C(mA)$	$V_{CB}(V)$	$I_C(mA)$	$V_{CB}(V)$	$I_C(mA)$

MODEL GRAPHS:

INPUT CHARACTERISTICS:



OUTPUT CHARACTERISTICS:



RESULT: The input and output characteristics of the transistor connected in common base configuration are obtained.

CE CHARACTERSTICS OF A TRANSISTOR

AIM: To obtain the input and output characteristics of transistor connected in common emitter configuration

APPARATUS:

1.NPN-Transistor	- BC107
2.Regulated Power supply	-(0-15V)
3.Resistors	-10KΩ, 1.5KΩ
4.Ammeter	-(0-200mA), (0-200μA)
5.Voltmeter	-(0-20V)

6.Breadboard Connecting wires

THEORY: A transistor is a three-terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and output is taken across the collector and emitter terminals. Therefore, the emitter terminal is common to both input and output.

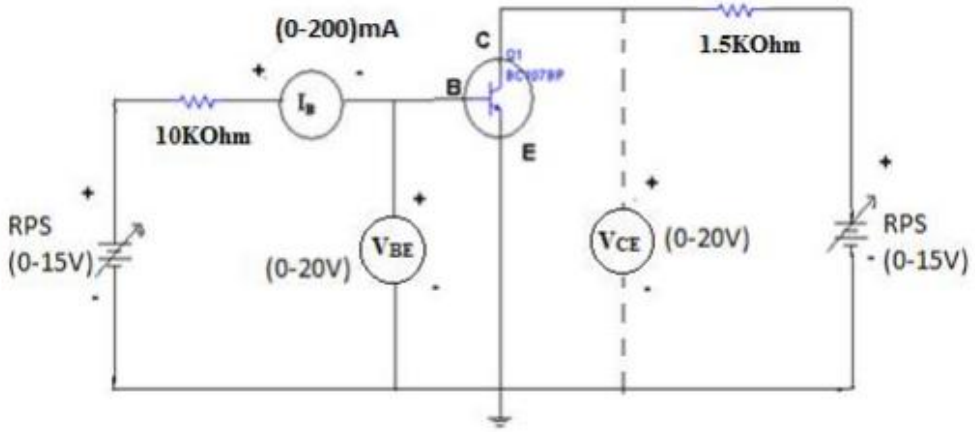
The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement I_B increases less rapidly with V_{BE}. Therefore, input resistance of CE circuit is higher than that of CB circuit.

The output characteristics are drawn between Ic and V_{CE} at constant IB. the collector current varies with V_{CE} unto few volts only. After this the collector current becomes almost constant, and independent of V_{CE}. The value of V_{CE} up to which the collector current changes with V_{CE} is known as Knee voltage. The transistor always operated in the region above Knee voltage, I_C is always constant and is approximately equal to I_B. The current amplification factor of CE configuration is given by

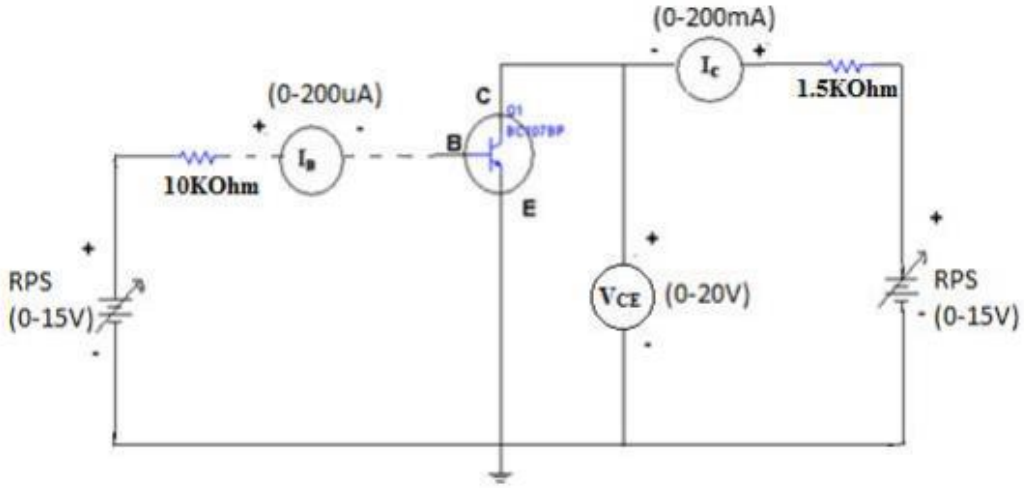
$$\mathbf{B = \Delta I_C / \Delta I_B}$$

CIRCUIT DIAGRAM:

INPUT CHARACTERISTICS:



OUTPUT CHARACTERISTICS:



PROCEDURE:

INPUT CHARECTERSTICS:

1. Connect the circuit as per the circuit diagram.
2. For plotting the input characteristics the output voltage VCE is kept constant at 0V and for different values of V_{BE}. Note down the values of IC
3. Repeat the above step by keeping VCE at 5V and 8V.
4. Tabulate all the readings.
5. Plot the graph between VBE and IB for constant VCE

OUTPUT CHARACTERSTICS:

1. Connect the circuit as per the circuit diagram

2. For plotting the output characteristics the input current I_B is kept constant at 10mA and for different values of V_{CE} note down the values of IC

3. Repeat the above step by keeping IB at 20μA, 60μA

4. Tabulate the all the readings 5. Plot the graph between V_{CE} and I_C for constant I_B

OBSERVATIONS:

INPUT CHARACTERISTICS:

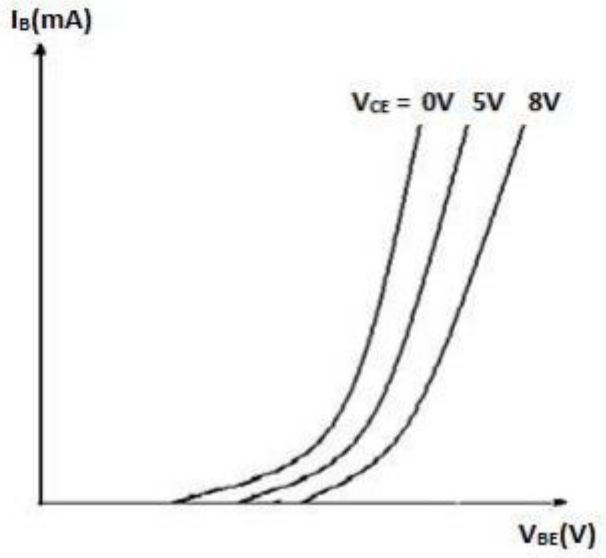
S.No	V_{CE} = 0V		V_{CE} = 5V		V_{CE} = 8V	
	V_{BE}(V)	I_B(mA)	V_{BE}(V)	I_B(mA)	V_{BE}(V)	I_B(mA)

OUTPUT CHARACTERISTICS:

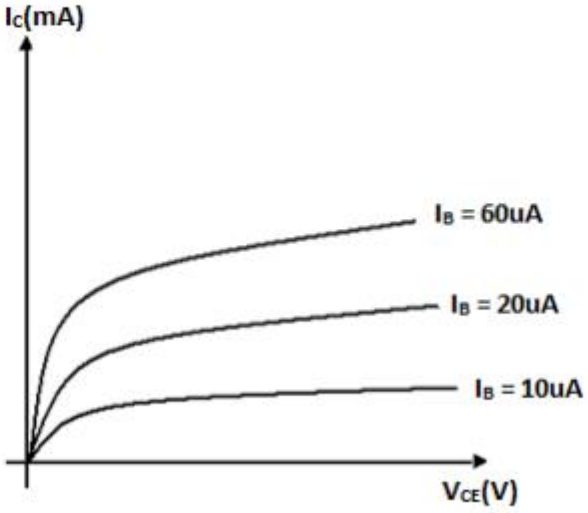
S.NO	I_B = 10 μA		I_B = 20 μA		I_B = 60 μA	
	V_{CE}(V)	I_C(mA)	V_{CE}(V)	I_C(mA)	V_{CE}(V)	I_C(mA)

MODEL GRAPHS:

INPUT CHARACTERSTICS:



OUTPUT CHARECTERSTICS:



RESULT: The input and output characteristics of a transistor in common emitter configuration are obtained

EXP No:5

FREQUENCY RESPONSE OF CE AMPLIFIER

AIM:

a. To measure the voltage gain of CE amplifier

b. To draw the frequency response curve of CE amplifier

APPARATUS:

1.Transistor	- BC107
2.Regulated Power Supply	-(0-15V)
3.Resistors	-10KΩ, 1KΩ, 4.7KΩ
4.Variable Resistor	-(0-100KΩ)
5.Capacitors	-22μF, 47μF
6.Voltmeter	-(0-20V)
7.Function Generator	
8.CRO	
9.Breadboard	
10.Connecting wires	

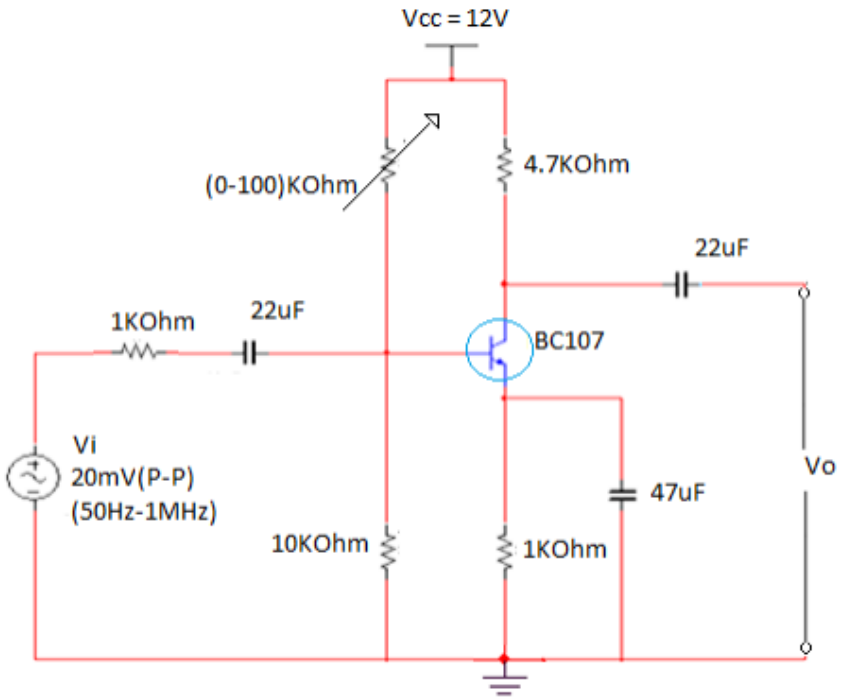
THEORY:

The CE amplifier provides high gain &wide frequency response. The emitter lead is common to both input & output circuits and is grounded. The emitter-base circuit is forward biased. The collector current is controlled by the base current rather than emitter current. The input signal is applied to base terminal of the transistor and amplifier output is taken across collector terminal. A very small change in base current produces a much larger change in collector current.

When +VE half-cycle is fed to the input circuit, it opposes the forward bias of the circuit which causes the collector current to decrease, it decreases the voltage more –VE. Thus, when input cycle varies through a -VE half-cycle, increases the forward bias of the circuit, which causes the collector current to increases thus the output signal is common emitter amplifier is in out of phase with the input signal.

CIRCUIT DIAGRAM:

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connect the circuit as shown in circuit diagram
2. Apply the input of 20mV peak-to-peak and 50Hz frequency using function generator.
3. Measure the Output Voltage VO (p-p).
4. Tabulate the readings in the tabular form.
5. The voltage gain can be calculated by using the expression Av= (V0/Vi)
6. For plotting the frequency response, the input voltage is kept Constant at 20mV peak-topeak and the frequency is varied from 50Hz to 1MHz Using function generator.
7. All the readings are tabulated and voltage gain in dB is calculated by using the expression Av=20 log10 (V0/Vi)
8. A graph is drawn by taking frequency on x-axis and gain in dB on y-axis on Semi-log graph. The band width of the amplifier is calculated from the graph using the expression,

Bandwidth, BW=f2-f1

Where f1 is the lower cut-off frequency of CE amplifier, and

Where f2 is the upper cut-off frequency of CE amplifier

The bandwidth product of the amplifier is calculated using the expression

Gain Bandwidth product = (3dB mid-band gain) X (Bandwidth)

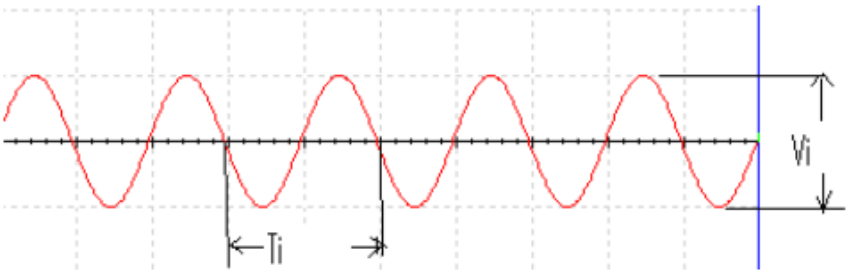
OBSERVATIONS:

FREQUENCY RESPONSE:

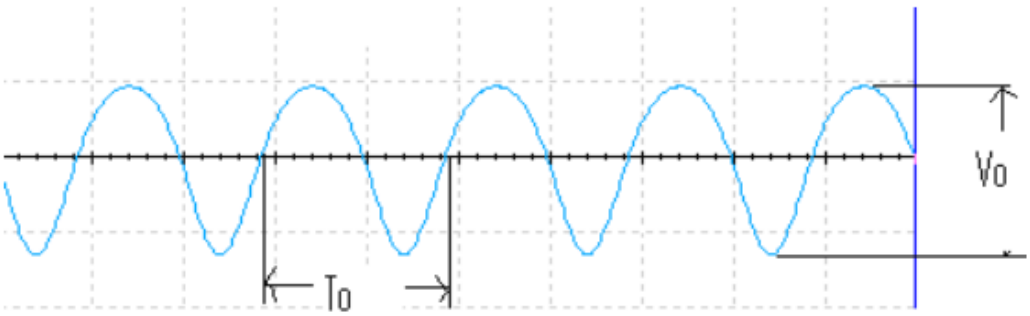
Frequency (Hz)	Input voltage (v_i)	Output voltage (v_0)	A_V	Gain in dB $A_v = 20 \log_{10}(v_0/v_i)$

MODEL WAVEFORMS:

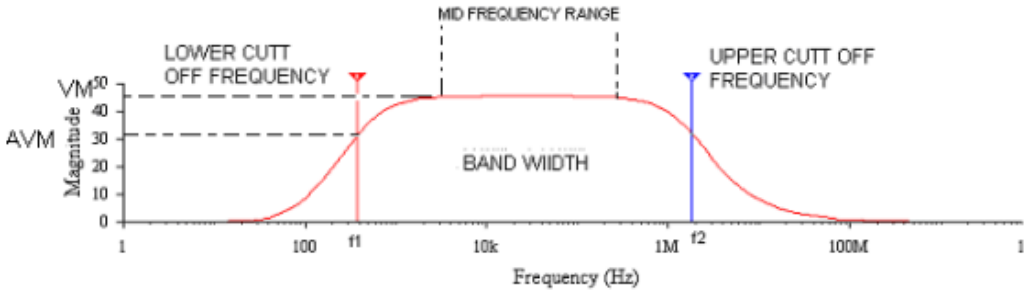
INPUT WAVEFORM:



OUTPUT WAVEFORM:



FREQUENCY RESPONSE:



RESULT: The voltage gain and frequency response of the CE amplifier are obtained.

EXP No:6

RC COUPLED AMPLIFIER

AIM:

1. To calculate voltage gain.
2. To observe frequency response of 2 stage RC coupled amplifier.

APPARATUS:

1.Transistor	- BC107
2.Regulated Power Supply	-(0-15V)
3.Resistors	-3.3KΩ, 33KΩ, 330Ω, 1KΩ, 4.7KΩ
4.Capacitors	-100µF, 10µF
5.Voltmeter	-(0-20V)
6.Function Generator	
7.CRO	
8.Breadboard	
9.Connecting wires	

THEORY:

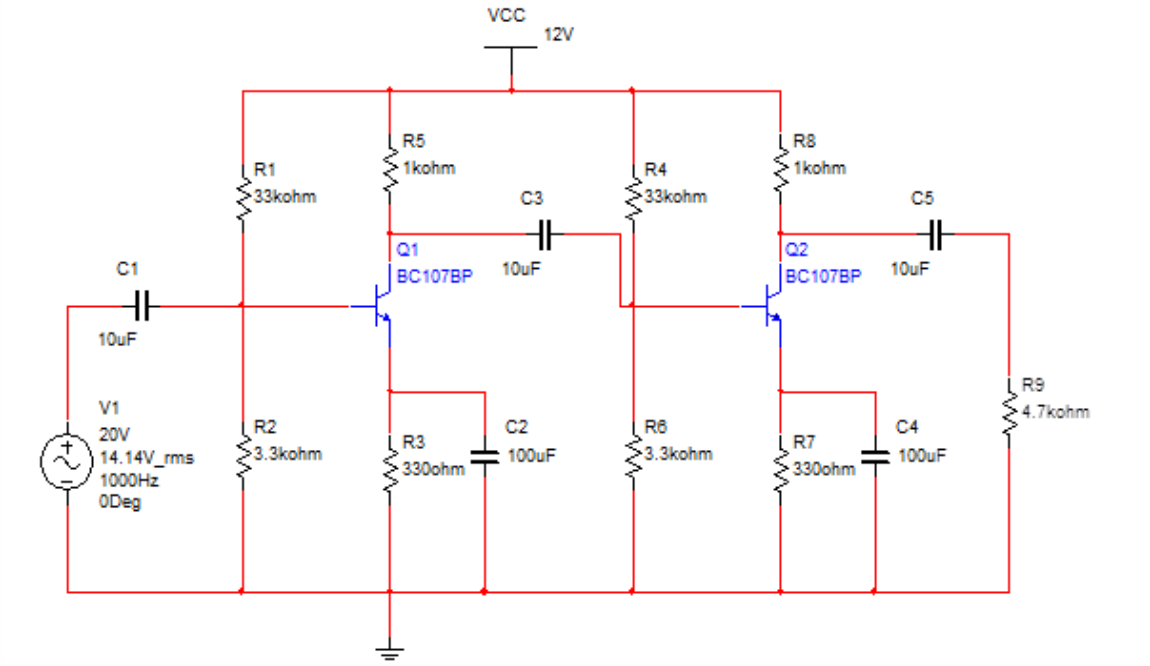
This is most popular type of coupling as it provides excellent audio fidelity. A coupling capacitor is used to connect output of first stage to input of second stage. Resistances R1, R2, RE form biasing and stabilization network. Emitter bypass capacitor offers low reactance paths to signal coupling Capacitor transmits ac signal, blocks DC. Cascade stages amplify signal and overall gain is increased total gain is less than product of gains of individual stages. Thus for more gain coupling is done and overall gain of two stages equals to A = A1 * A2

A1 = voltage gain of first stage

A2 = voltage gain of second stage.

When ac signal is applied to the base of the transistor, its amplified output appears across the collector resistor RC. It is given to the second stage for further amplification and signal appears with more strength. Frequency response curve is obtained by plotting a graph between frequency and gain in dB .The gain is constant in mid frequency range and gain decreases on both sides of the mid frequency range. The gain decreases in the low frequency range due to coupling capacitor CC and at high frequencies due to junction capacitance C_{BE}.

CIRCUIT DIAGRAM:



PROCEDURE:

1. Apply input by using function generator to the circuit.
2. Observe the output waveform on CRO.
3. Measure the voltage at

a. Output of first stage

b. Output of second stage.

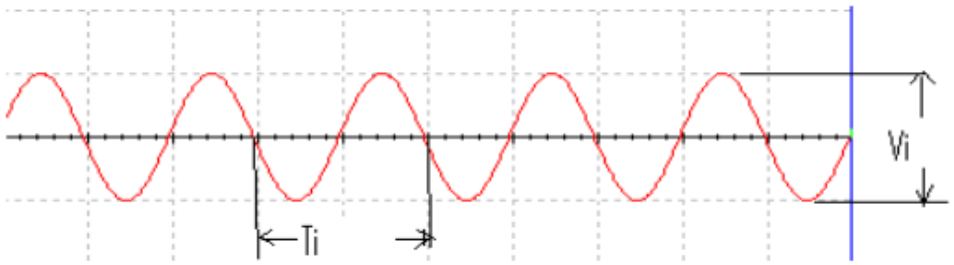
4. From the readings calculate voltage gain of first stage, second stage and overall gain of two stages. Disconnect second stage and then measure output voltage of first stage and calculate voltage gain.
5. Compare it with voltage gain obtained when second stage was connected.
6. Note down various values of gain for different frequencies.
7. A graph is plotted between frequency and voltage gain.

OBSERVATIONS:

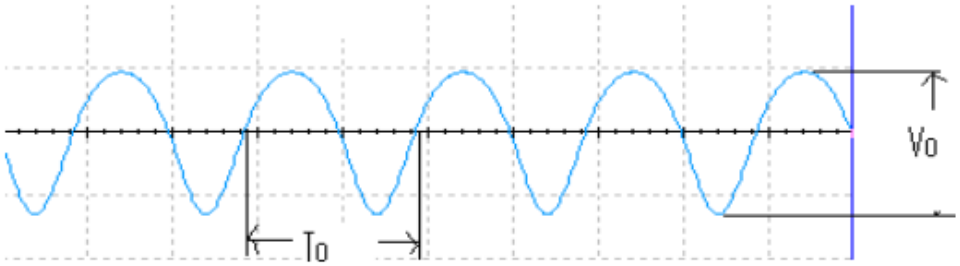
S. No	Frequency (Hz)	I/P Voltage (V_i)	O/P Voltage (V_o)	A_V	Voltage Gain $A_V = 20 \log_{10}(V_o/V_i)$ dB

MODEL WAVEFORMS:

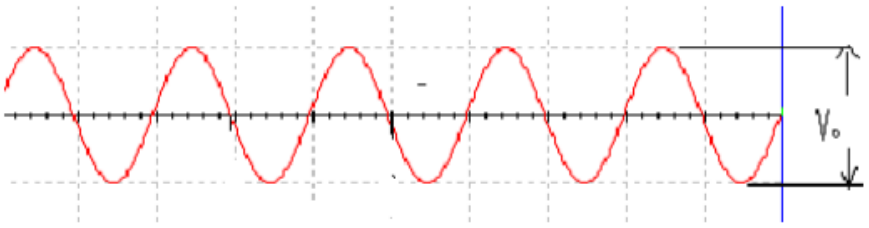
INPUT WAVEFORM:



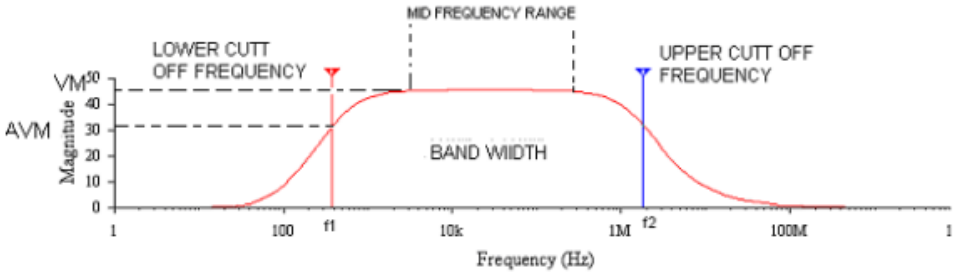
FIRST STAGE OUTPUT:



SECOND STAGE OUTPUT:



FREQUENCY RESPONSE:



RESULT: Thus, voltage gain is calculated and frequency response is observed.

EXP No:7

VERIFICATION OF LOGIC GATES

AIM: To study and verify the truth table of logic Gates. Two input (i) OR (ii) AND (iii) NOT (iv) NOR (v) NAND (vi) EXCLUSIVE OR (vii) EXCLUSIVE NOR

APPARATUS:

1. DIGITAL IC TRAINER KIT.
2. IC 7408, IC 7404, IC 7400, IC 7432, IC 7406, IC 7402, IC 7486
3. CONNECTING WIRES/PATCH CARDS.

THEORY:

In the digital circuits, two discrete voltages are recognized as two logic levels, logic '1' and Logic '0'. These are also known as 'high' and 'low' logic levels. Circuits that process digital signal and take logical decisions are called logic gates. Each gate has two or more inputs and one output Terminal. The output wave form at any instant depends only upon the input waveform at that Instant. Such circuits are called combinational logic circuit. The logic gates transistor logic (RTL), diode transistor logic (DTL), transistor transistor logic (TTL) and emitter coupled Logic (ECL). The last two types are in wide use and are available in ic version. The three basic Logic gates are or gate, and gate, and not gate.

AND-GATE:

AND gate has two or more inputs and only one output. If the both the inputs are 1 the output is 1. If any one of the inputs is 0 the output is 0. Thus, the output of the AND gate is equal to the product of the input. The output can be expressed Y=A.B.

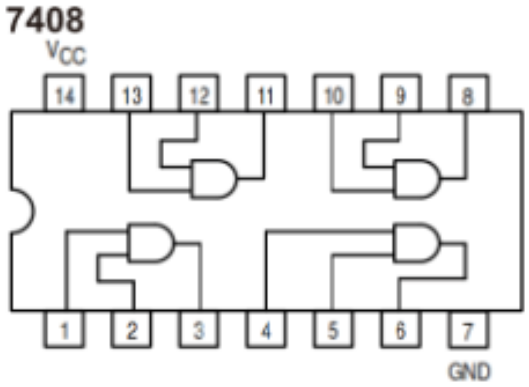
OR-GATE:

OR gate has two or more inputs and only one output. If the both the inputs are 1 the output is 1. When both of the inputs are 0 the output is 0. Thus, the output of the OR gate is equal to the sum of the input. The output can be expressed as Y=A+B.

Pin Diagrams and Their Truth Tables:

AND Gate

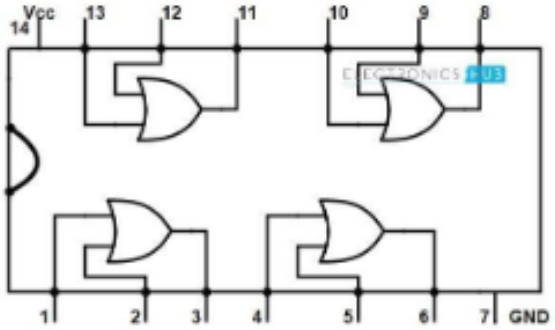
TRUTH TABLE



AND		
A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate: 7432

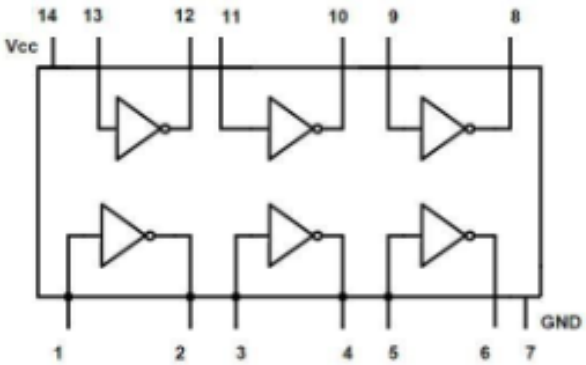
TRUTH TABLE



OR		
A	B	Y=A.B
0	0	0
0	1	1
1	0	1
1	1	1

NOT Gate: 7404

TRUTH TABLE



NOT Gate	
A	Y=A'
0	1
1	0

NOT-Gate:

A NOT gate has only one input and one output. The NOT gate is also known as an Inverter Gate or Complement. The output of the not gate is complement of input. The output can be Expressed as Y=A'

NAND-Gate:

NAND gate has two or more inputs and only one output. The NAND operation also be performed if a combination of an AND gate and a NOT gate. If any one of the input is 0 is the output is 1. In all other cases the output is 0. The output can be expressed as Y=A.B.

NOR-Gate:

NOR gate has two or more inputs and only one output. The NOR operations can also be Performed if a combination of an OR gate and a NOT gate. If any one of the input is 1 is the Output is 0. In all other cases the output is 1. The output can be expressed as Y=A+B.

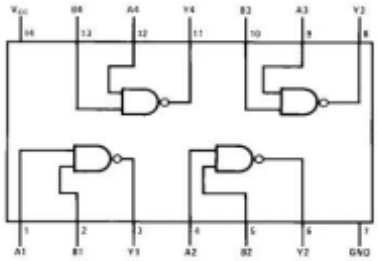
EX-OR Gate:

The output of an Exclusive-OR gate ONLY goes "HIGH" when its two input terminals are at "DIFFERENT" logic levels with respect to each other. An odd number of logic "1's" on its inputs gives logic "1" at the output. These two inputs can be at logic level "1" or at logic level "0" giving us the Boolean expression of: $Q = (A \oplus B) = \overline{A}.B + A.\overline{B}$

EX-NOR Gate:

Basically the "Exclusive-NOR" gate is a combination of the Exclusive-OR gate and the NOT gate but has a truth table similar to the standard NOR gate in that it has an output that is normally at logic level "1" and goes "LOW" to logic level "0" when ANY of its inputs are at logic level "1". However, an output "1" is only obtained if both of its inputs are at the same logic level, either binary "1" or "0". For example, "00" or "11". This input combination would then give us the $Q = \overline{A}.\overline{B} + A.B$

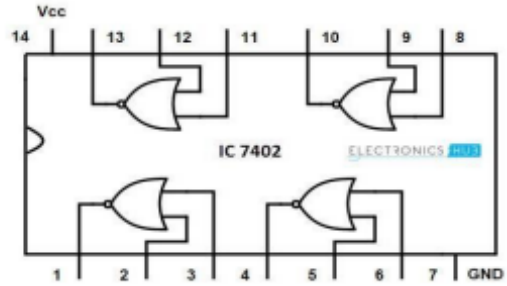
NAND gate: 7400



TRUTH TABLE

NAND gate		
A	B	Y=
0	0	1
0	1	1
1	0	1
1	1	0

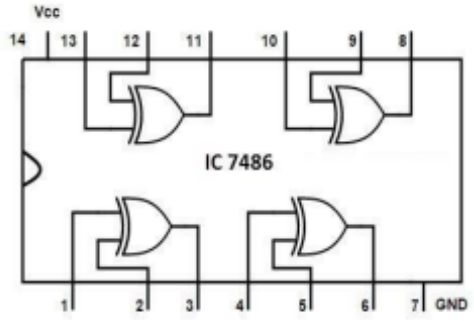
NOR Gate: 7402



TRUTH TABLE

NOR Gate: 7402		
A	B	Y=
0	0	1
0	1	0
1	0	0
1	1	0

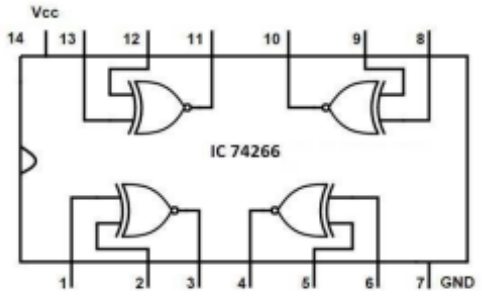
EX-OR Gate:7486



TRUTH TABLE

EX-OR Gate		
A	B	Y=
0	0	0
0	1	1
1	0	1
1	1	0

EX-NOR Gate: 74266



TRUTH TABLE

EX-NOR Gate		
A	B	Y=
0	0	1
0	1	0
1	0	0
1	1	1

Procedure:

1. Check the components for their working.

2. Insert the appropriate IC into the IC base.

3. Make connections as shown in the circuit diagram.

4. Provide the input data via the input switches and observe the output on output LEDs

5. Tabulate the values for different input combinations.

Result:

Truth table of various logic function (OR, NOR, NOT, AND, NAND, EX-OR GATE) are verified.

EXP No:8

VERIFICATION OF FLIPFLOPS

AIM: To verify of state tables of various flip-flops using NAND & NOR gates.

APPARATUS:

1.FLIPFLOP Trainer Kit
2.Patchcards

THEORY:

A Flip flop is a bistable electronic circuit that has two stable states. That is, its output is either +5V (logic 1) or 0V (logic 0). A Flip Flop can be referred as memory device since its output will remain unchanged until its input is not changed. It is used to store one binary digit.

R-S FLIP FLOP: A R-S Flip Flop is one that has two inputs R & S and two outputs Q & Q'. An R-S Flip Flop can be constructed using NOR gates or NAND gates. Figure shows R-S Flip Flop constructed using four NAND gates.

D- FLIP FLOP: To avoid the forbidden case that occur in R-S Flip Flop, when R=S=1, D Flip Flop is implemented. In the D Flip Flop, there is only one input D as show in figure. We can transmit the value of D at the output of the Flip Flop when CLK is high.

J-K FLIP FLOP: Setting R=S=1 with a R-S Flip Flop Q and Q‟ will set to the same logic level. This is an illegal condition. The J-K Flip Flop accounts for this illegal input. It is used to build counter. The values of J and K determine what a J-K Flip Flop does on the next clock edge. When both are low, the Flip Flop retains its last state. When J is low and K is high, the Flip Flop resets. When J is high and K is low, the Flip Flop sets. When both are high the Flip flop toggles. In this last mode, the J-K Flip Flop can be used as a frequency divider.

T- FLIP FLOP: The T- Flip Flop is known as Toggle Flip flop. The T Flip flop is a modification of the JK Flip flop by connecting both inputs J and K together. Figure shows the logic diagram of T flip flop, logic symbol and truth table of T Flip flop is also shown.

When T=0, both AND gates are disabled and hence there is no change in the previous output. When T=1(J=K=1) output toggles. Toggles means that the output is 0 when the previous state is 1 otherwise output is 1 when the previous state is 0. So the output is a complement of the previous output.

CIRCUIT DIAGRAM:

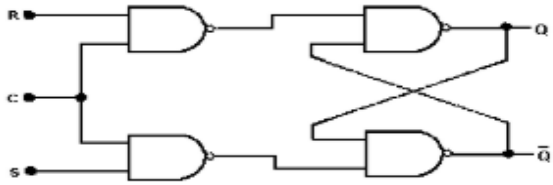
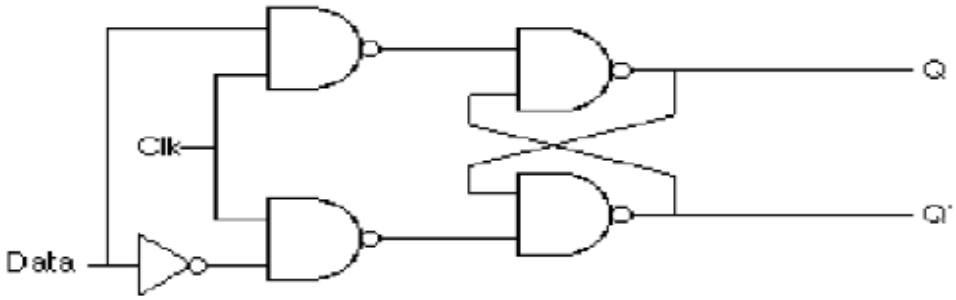


Fig (i) R-S FLIP–FLOP

CHARACTERISTIC TABLE

CLK	S	R	Q (t+1)
0	X	X	NO CHANGE
1	0	0	NO CHANGE
1	0	1	0
1	1	0	1
1	1	1	FORBIDDEN

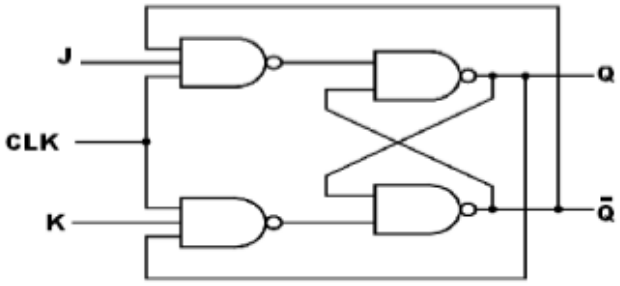
CIRCUIT DIAGRAM



OBSERVATION TABLE: D - FLIP –FLOP

CLK	D	Q (t+1)
0	X	NO CHANGE
1	1	1
1	0	0

CIRCUIT DIAGRAM:-



OBSERVATION TABLE: J-K - FLIP -FLOP

CLK	J	K	Q (t+1)
0	x	X	NO CHANGE
1	0	0	NO CHANGE
1	0	1	0
1	1	0	1
1	1	1	TOGGLE

Table (iii) Characteristic table of J-K Flip-Flop

Circuit Diagram

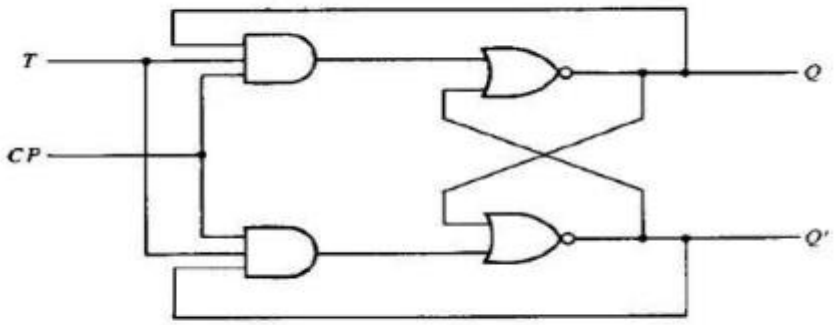


Fig (iv) Circuit diagram of JK Flip Flop

OBSERVATION TABLE: T - FLIP -FLOP

Preset State	Flip flop Input	Next State
Qn	T	Qn+1
0	0	0
0	1	1
1	0	1
1	1	0

PROCEDURE:

1. Connections are made as per circuit diagram.
2. Change the combinations of inputs &
3. Verify the truth table for various combinations of inputs.

PRECAUTIONS:

1) All Connections should be according to circuit diagram.
2) All Connections should be right and tight.
3) Reading should be taken carefully.
4) Switch off Power supply after completing the Experiment.

RESULT: The observation tables of various flip-flops are verified